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... of objects associated with the configuration instructions, a parameter ... File Generated by the Configuration Definition Module ... Select group type to create -\ QQ2 ...

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A Appendix: Abbreviations

... , CIS Computing, C Object, CP Approximation, CP ... - Computational Many-Particle Physics, 2007 -

generate configuration instruction template package library object - GoogleSc... .

books.google.com

... interval, 67, 102 configuration interaction method ... 375 instruction throughput, 686
instruction-level parallelism ... random numbers congruential generator, 68 Gauss ...

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Core template package for creating run-time reconfigurable cores

CD Patterson - US Patent 7,143,418, 2006 - Google Patents

... to generate a netlist 103 for the design, importing ... Once the configuration data has
been produced, the ... Each template class 65 The instructions in executable ...

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[CITATION] VersaCAD: A Viable CADD Package For Undergraduate CADD Instruction?

MJ Miller, RA Wilke, O Columbus - Proceedings - American Society for Engineering Education

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... of objects associated with the configuration instructions, a parameter ... File Generated
by the Configuration Definition Module ... Select group type to create -\ QQ2 ...

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**Object-oriented system, method and article of manufacture for a client-server application
enabler ...**

generate configuration instruction template package library object - Google Sc... .

SL Gish... - US Patent 5,768,510, 1998 - freepatentsonline.com

... The developer will create these handler functions and ... tools for application installation and configuration are provided ... A Java startup applet template is also ...

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Method and apparatus for distributing templates in a component system

JJ Buxton - US Patent 6,195,794, 2001 - freepatentsonline.com

... 5838918, Distributing system configuration information from a ... template builder 400
to create a distribution ... illustrated flow chart into instructions or objects ...

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Integrating GNAT and GCC

R Kenner - Proceedings of the conference on TRI-Ada'94, 1994 - portal.acm.org

... and are efficient, Parameters relating to register configuration are also ... Instruction scheduling (second pass ... into GCC types in order to generate efficient code ...

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Key authors: T Veldhuizen - S Gish - J Siek - J Ribeiro Filh... - D Gannon



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M Behm, J Ludden, Y Lichtenstein, M Rimón, M Vinov ... - Proceedings of the 41st Design Automation Conference (DAC' ... , 1920 - [doi.ieeecomputersociety.org](#)

... can leave prop- erties completely unspecified, provide them ... Genesys-Pro to generate instruction streams for ... processor/thread in a multiprocessor configuration. ...

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[Method for determining the impact on test coverage of scan chain parallelization by analysis of a ...](#)

JR Rearick, M Sharma - US Patent 7,139,948, 2006 - Google Patents

... including a serial scan chain; and generating a second ... E@I. The serial scan chain configuration of FIG. ... bit patterns are reviewed to determine ifthe specified ...

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ME Miller, BL Chamberlin, MD Lewis, SH Blackmore - US Patent App. 10/611,688, 2003 - Google Patents

... of objects associated with the configuration instructions, a parameter ... File Generated by the Configuration Definition Module ... Select group type to create -\ QQ2 ...

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[Adaptive test program generation](#)

A Adir, R Emek, E Marcus - US Patent App. 10/040,940, 2002 - Google Patents

... By appropriate configuration, it is possible for test program ... the input to the test program generator is a ... resource, and even the type of the instruction to be ...

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[System for evaluating performance of a combined-cycle power plant](#)

ST Adelman, RR Gay - US Patent 6,591,225, 2003 - [freepatentsonline.com](#)

... media that may contain computer instructions that implement ... a run module 907 , a generate equation module ... the user to specify the configuration and economic ...

[Cited by 4](#) - [Related articles](#) - [Web Search](#) - [All 3 versions](#)

[Algorithm-to-hardware system and method for creating a digital circuit](#)

RJ Carter - US Patent App. 10/051,078, 2002 - Google Patents

... that can be used to determine a configuration ... 100 is not limited to creating the configuration instructions for re ... 100 is additionally operable to create a chip ...

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[DVGen: a test generator for the transmeta efficeon VLIW processor](#)

KD Rich, SG Govindaraju, R Shaw, D Dobrikin - High-Level Design Validation and Test Workshop, 2005. Tenth ... , 1930 - [ieeexplore.ieee.org](#)

... branches in Efficeon, trap instructions were used ... the corresponding option not to generate such situations. ... different bugs are uncovered in each configuration. ...

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[Genesys-Pro: Innovations in Test Program Generation for Functional Processor Verification -](#)

